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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/293,563	04/15/1999	RONALD P. BIANCHINI	FORE-43	5047

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EXAMINER
NGUYEN, STEVEN H D

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/293,563	BIANCHINI, RONALD P.	
	Examiner	Art Unit	
	Steven HD Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-2, 15-16 and 18-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Tout (USP 5991295).

Regarding claim 1, Tout discloses (Fig 1-8 and col. 1, lines 8 to col. 10, lines 2) a switch system (Fig 1, Ref 2) comprising at least one input port mechanisms (Fig 2, Ref Port) for receiving the packets; at least one output port mechanisms (Fig 2, Ref Port) for transmitting the packets; a carrier mechanism (Fig 2, ref 10) which connects to each input port mechanism and each output port mechanism for conveying the packets; a memory mechanism (Fig 2, Ref 8) which connects to the carrier mechanism, stores the packets and a mechanism for providing packets to the memory mechanism through the carrier mechanism from the input port mechanisms, said providing mechanism able to transfer packets or portions of packets whose

total width equals the width of the carrier mechanism in each transfer cycle to the memory mechanism (Fig 5 and Fig 2, Ref 6 which is a controller for providing the packets to the memory 8 in each transfer cycle where the bus between the input port and memory has a width which is equal to a portion of packet) and a width of carrier mechanism (Fig 2, Ref 10 has a width 8 bit and input and port mechanism is serial) is wider than the width of input and output port mechanism.

Regarding claim 2, Tout discloses the width of the carrier mechanism is independent of the width of any packet (Col. 5, lines 63, the width of the bus is independent with the width of any packet because packet has 54 bit and bus has 8 bit).

Regarding claim 15, Tout disclose (Fig 1-8 and col. 1, lines 8 to col. 10, lines 2) a switch comprising a central resource (Fig 2, Ref 6) having a width and an overall bandwidth and input port mechanisms and output port mechanisms each having widths for receiving or sending packets, respectively, said central resource partitioned via time slots that are allocated to the input and output port mechanisms, said central resource width independent of any input or output port mechanisms width and the overall bandwidth can grow without limitation by input or output port mechanism width (Col. 3, lines 64 to col. 4, lines 27, the data controller will allocate the bandwidth according the demand of the I/O port and the resource is partition into the time slots for I/O); and a memory mechanism for storing packets, said memory mechanism connected to the central resource (Fig 2, Ref 8).

Regarding claim 16, Tout discloses the central resource includes a memory bus (Fig 2, Ref 17).

Regarding claim 18, Tout discloses (Fig 1-8 and col. 1, lines 8 to col. 10, lines 2) a switch comprising a time division multiplex bus (Fig 2, Ref 10); a memory mechanism connected to the bus which is accessed via time division multiplexing of the bus (Fig 2, Ref 8); and a mechanism for reading and writing data of packets to the memory mechanism through the bus without knowledge of the packet boundaries of the data (col. 5, lines 35-51, the memory will write a portion of data packet into the memory without knowledge of the boundary of the packet).

Regarding claim 19, Tout discloses (Fig 1-8 and col. 1, lines 8 to col. 10, lines 2) a switch comprising a time division multiplex carrier mechanism having a width (Fig 2, ref 10); a memory mechanism (Fig 2, Ref 8) connected to the carrier mechanism; and an input stage mechanism having a width for providing data of packets to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple of the input stage mechanism width (Col. 3, lines 64 to col. 5, lines 10).

Regarding claims 20-21, Tout discloses (Fig 1-8 and col. 1, lines 8 to col. 10, lines 2) a switching packets comprising receiving a first packet and at least a second packet at a switch mechanism (Fig 2, Ref 7 and 5); and transferring data of the first packet and the second packet to a memory mechanism (Fig 2, ref 8) via time division multiplexing (Fig 2, Ref 10) of a bus having a width so data from the packets fills a predetermined portion of the width of the bus, said bus width not necessarily a function of the data contained in any packet; the bus width is a positive non-integer multiple of the packet size (Col. 3, lines 64 to col. 5, lines 10).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-12, 14, 17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tout as applied to claims 1, 15 and 20 above, and further in view of Fukano (USP 5774453).

Regarding claims 3-4, Tout does not disclose the claimed invention. However, an examiner takes an official noticed that a method and apparatus for transmitting/receiving a variable sized packets are well known and expected in the art at the time of invention was made. The motivation would have been to support a frame relay network.

Regarding claim 5, Tout discloses the providing mechanism also provides packets from the memory mechanism to the output port mechanisms through the carrier mechanism, said providing mechanism transferring packets or portions of packets whose total data equals the width of the carrier mechanism in each transfer cycle from the memory mechanism (Fig 5 and Fig 2, Ref 6 which is a controller for providing the packets to the memory 8 in each transfer cycle where the bus between the input port and memory has a width which is equal to a portion of packet).

Regarding claims 6-9, Tout fails to disclose the claimed invention. However, Fukano discloses (Fig 1-2 and col. 1, lines 6 to col. 7, lines 63) the providing mechanism includes input

stage queue groups (Fig 1, Ref 11) connected to the carrier mechanism and the input port mechanisms for storing packets received by the input port mechanisms, and output stage queue groups (Fig 1, Ref 16) connected to the providing mechanism and the output port mechanisms for storing packets to be sent out the output port mechanisms (Fig 1); the providing mechanism includes a classifying mechanism which places a packet which is received by the input port mechanism into a corresponding queue group, said classifying mechanism connected to the input port mechanisms and the input stage queue groups (Fig 1, Ref 11 discloses a classified mechanism for classifying the packets into a queue group); a processing mechanism which places a packet in an output stage queue group into a corresponding output port mechanism, said processing mechanism connected to the output port mechanisms and the output stage queue groups (Fig 1, ATM switch has a processing means for placing the packets into a corresponding of output queue); the classifying mechanism (Fig 1, Ref 11 has a classifier for inputting a packet in a corresponding queue) includes a first write finite state machine for writing packets into a corresponding input stage queue, the providing mechanism includes a second write finite state machine for writing packets from an input stage queue group into the memory mechanism (Fig 1, ref 13 discloses the packets in the input queue are transferred to the shared memory) , and a first read finite state machine for reading packets from the memory mechanism to an output stage queue group, and the processing mechanism includes a second read finite state machine for reading a packet from the output stage queue group to the network (Fig 1, ref 18 has a read port for reading the packets in the shared memory into the corresponding queues of the output port) and the first read finite state machine only transfers data of packets of an input stage queue group

to the bus when the input queue group contains at least one cache-line of data (See Fig 1, the input buffer will transmit the packet to the bus when it has a data).

Since, Tout suggests a memory being divided into the queues wherein each queue stores a classified packet. Therefore, it would have been obvious to one of ordinary skill in the art for apply a buffer into an input port for storing the packet before transferring into a shared memory of the switch as disclosed Fukano's switch into Tout's switch. The motivation would have been to prevent a collision.

Regarding claim 10, Tout discloses the memory mechanism includes a shared memory (Fig 2, ref 8).

Regarding claim 11, Tout discloses packets or portions of packets travel on the carrier mechanism based on time division multiplexing (Fig 2, Ref 10).

Regarding claim 12, Tout discloses the carrier mechanism includes a bus (Fig 2, Ref 10).

Regarding claim 14, Tout discloses the communication line is an ATM network (col. 3, lines 17-24).

Regarding claim 17, Tout fails disclose the claimed invention. However, Fukano discloses (Fig 1-2 and col. 1, lines 6 to col. 7, lines 63) the central resource includes queue groups in which packets are classified, and the packets are read from and written into the memory mechanism from the queue groups (Fig 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply an input buffer for storing the classified packet into the queue group as disclosed by Fukano into Tout's switch. The motivation would have been to reduce the latency of higher priority packet and prevent a dead lock in the switch.

Regarding claim 22, Tout fails to disclose the claimed invention. In the same field of endeavor, Fukano discloses (Fig 1-2 and col. 1, lines 6 to col. 7, lines 63) the steps of placing the first packet and at least the second packet in an input stage queue group (Fig 1, Ref 11); and transferring data in the input stage queue group during an allocated time slot on the bus to the memory mechanism so the data fills the predetermined portion of the width of the bus (Fig 1, Ref 13, the packet in the input buffer will be transferred to the memory of the switch).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply an input buffer for storing the classified packet into the queue group as disclosed by Fukano into Tout's switch. The motivation would have been to reduce the latency of higher priority packet and prevent a dead lock in the switch.

5. Claims 13 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tout and Fukano as applied to claims 1 and 20 above, and further in view of Lyons (USP 5574505).

Regarding claims 13 and 23-24, Tout and Fukano fail to disclose the claimed invention. However, Lyons discloses a before the transferring data step there is the step of determining that the input-stage queue group has at least enough data to fill the predetermined portion of the width of the bus before data is transferred to the bus and before the transferring data step, there is the step of determining that the input stage queue group has at least one-cache line of data (Col. 2, lines 30-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a method of determining if an input buffer has a stored data and enough bytes to fill the slot as disclosed by Lyons' method into the method of Tout and Fukano. The motivation would have been to prevent data loss.

Response to Arguments

6. Applicant's arguments filed 9/11/2002 have been fully considered but they are not persuasive.

In response to pages 6-8, the applicant states that Tout does not disclose "said providing mechanism able to transfer packets or portion of the packets whose total width equals the width of the carrier mechanism in each cycle to the memory mechanism" and "said carrier mechanism having a width wider than the width of the input port and output port mechanism". In reply, Tout discloses the bus width "8 bits" of the input and output port is less than a bus width of interface between the memory 8 "memory mechanism", controller 6 "carrier mechanism" for transmitting the block of data from an input port to the memory 8 having a width "112 bits which equal 14 bytes" at "14 bytes bus" wherein the bock of data will equal to the wide of controller 6 in each transfer cycle. The portion of packet is read on "quarter cell, see col. 7, lines 64 to col. 8, lines 9 wherein the input pot has a width 8 bit, the controller and memory have a bus 14 bytes to transfer a quarter cell having 14 bytes width bus" (See col. 2, lines 7-35 and col. 8, lines 52-62) and as set forth of paragraph 1.

In response to claim 2, the applicant states that Tout does not disclose the width of the carrier mechanism is in dependent of the width of packet. In reply, the bus width of the controller 6 is independent from the width of packet because the bus has 14 bytes width and width of the packet is ATM cell.

In response to claim 15, the applicant states that Tout does not disclose the claimed invention. In reply, Tout clearly discloses the claimed invention as set forth at paragraph 2.

In response to claim 18, the applicant states that Tout does not disclose "a mechanism for reading and writing data of packets to the memory mechanism through the bus without knowledge of the packet of boundaries of the data. In reply, Tout disclose a mechanism for reading and writing the 14 bytes of the data packet to the memory mechanism. Therefore, it does not care about the boundary of the packet when it reads and writes the packets to or from the memory.

In response to claim 19, the applicants states Tout does not disclose "an input stage mechanism having a width for providing data of packets to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple of the input stage mechanism width". In reply, Tout discloses the input stage "input port, Fig 1, Ref port, 155 Mbps" for receiving the data of packets and providing a data of packet via a time division multiplexing bus having 5 time slots "800 Mbps" and input port has a width of a time slot (Col. 3, lines 64 to col. 5, lines 10).

In response to claims 20-21, the applicant states that Tout does not disclose "the bus width not necessarily a function of the data contained in any packet". In reply, Tout discloses the bus width is not a function of data contained in any packet because the bus width used to carrier ATM via a 4 time slot so the bus width is not function of data contain in any packet because a time slot does not carrier all data of packet and bus width is positive non interger multiple of the packet size greater than one (bus width is greater than packet size, the bus has five time slot). So the bus width is not a function of data contained in a packet because the bus width is independent from data of any packets.

In response to pages 11-17, the applicant states that Tout and Fukano do not disclose the claimed invention. In reply, Tout discloses the bus width "8 bits" of the input and output port is less than a bus width of interface between the memory 8 "memory mechanism", controller 6 "carrier mechanism" for transmitting the block of data from an input port to the memory 8 having a width "112 bits which equal 14 bytes" at "14 bytes bus" wherein the bock of data will equal to the wide of controller 6 in each transfer cycle. The portion of packet is read on "quarter cell, see col. 7, lines 64 to col. 8, lines 9 wherein the input pot has a width 8 bit, the controller and memory have a bus 14 bytes to transfer a quarter cell having 14 bytes width bus" (See col. 2, lines 7-35 and col. 8, lines 52-62).

In response to applicant's argument that Tout and Fukano are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Tout discloses a method and apparatus for transferring the input cell stream via a switch having a TDM bus and a shared memory for storing the input cell stream and Fukano discloses an ATM switch has plurality of input ports for receiving the cell stream and storing in the input buffer before transferring to the shared memory. Therefore, Tout and Fukano are same field of endeavor.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the

time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The teaching of Tout, Fukano and Lyons perform the claimed invention. Therefore, the rejection maintains.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

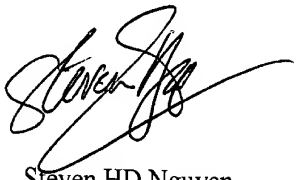
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (703) 308-8848. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on (703) 308-6602. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.



Steven HD Nguyen
Primary Examiner
Art Unit 2665
November 30, 2002